"T" network design and analysis using a programmable calculator

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ONE of the more popular networks used in the tank circuits of transistor power amplifiers is the "T" network (Fig 1), but calculation of the component values from the circuit equations, while fairly straightforward, is rather cumbersome, particularly if the calculations have to be repeated for several different sets of conditions. A further complication is that the transistor parameters needed for the calculations have to be in series form, whereas the data are usually available in parallel form, so that a parallel-to-series conversion has to be carried out. Table 1 shows the step by step procedure for designing a "T" network.

A disadvantage of the "T" network is that it is a narrow band circuit. If it is necessary to operate the amplifier over a wide range of frequencies, as would be the case on, say, 28MHz, then it will be necessary to provide some adjustment capability. In the usual arrangement the inductor is made constant and capacitors C1 and C2 are varied to maintain the correct impedance transformation as frequency is varied. C1 and C2 will also need to be varied to cope with the tolerances associated with all of the other parameters, eg the transistor output capacitance, the inductor value, load resistance etc.

Although satisfactory impedance transformation can be achieved over a wide range of conditions, it will be necessary to establish the range of values required for C1 and C2 so that suitable components can be chosen. Similarly, the circuit Q will vary as the conditions are varied, and it is necessary to ensure that its value does not become either too high or too low.

It is possible to carry out all the calculations required for both design and analysis by manual methods, but this is very time consuming and laborious. What usually happens is that the circuit values are calculated for a single set of conditions, and then cut-and-try methods are used on a prototype in an attempt to establish the optimum component values. However, the advent of the programmable calculator has provided an economic means by which repetitive and complex calculations may be carried out rapidly and easily.

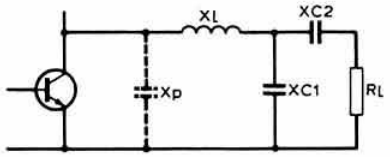

Fig 1. "T" network circuit diagram

This article presents two programs; the first allowing the values of XL, XC1 and XC2 to be calculated given the transistor parameters, the load resistance and the circuit Q required. Analysis of the circuit to assess the effects of parametric variations can be carried out using the second program.

Design program

The flow chart for the design program is shown in Fig 2. The reference figures to the right of each block relate to the program listing (see later). Provision has been made for the transistor data to be entered either in parallel or in series format. Usually the data are available in parallel form for output parameters and in series form for input parameters. In both cases the reactive element of the impedance must be entered as a reactance, not as a capacitance or inductance. Also, the sign of the reactance, ie negative for capacitive and positive for inductive, must be included.

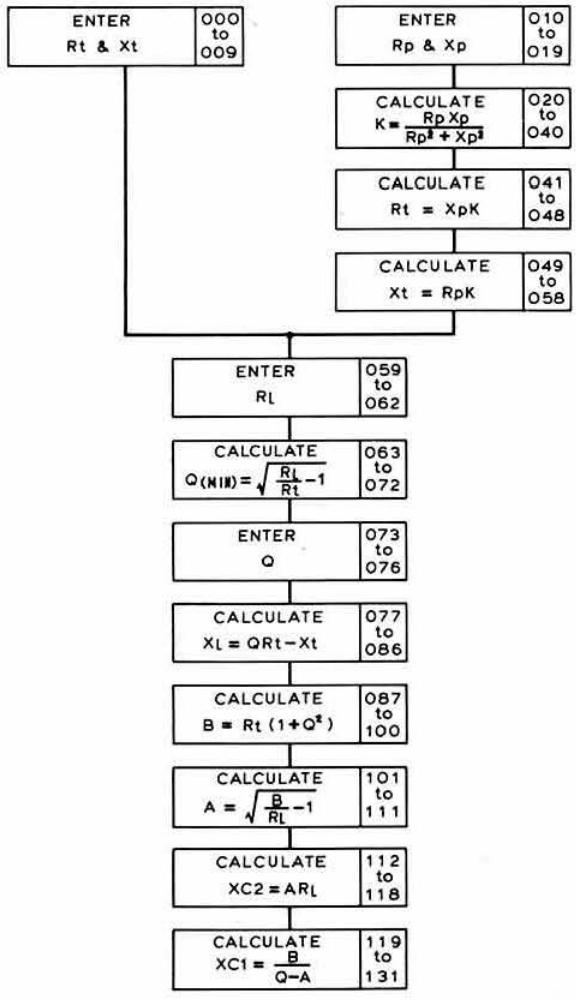

Fig 2. Design program flow chart

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Table 1. "T" network design procedure

1. Establish the transistor output capacitance from the data sheet and calculate the reactance at the required frequency (Xp).
2. Calculate Rp from $Rp = \frac{(VS - V_{CE(SAT)})^2}{2W}$ where W is the output power required.
3. Calculate Rt and Xt (the series equivalents of Rp and Xp) from
$$Rt = \frac{RpXp^2}{Rp^2 + Xp^2}$$
$$Xt = \frac{Rp^2Xp}{Rp^2 + Xp^2}$$
4. Calculate Q minimum from $Qmin = \sqrt{\frac{RL}{Rt} - 1}$ where RL is the antenna load impedance. Check that Qmin is less than the Q required and that Rt is not greater than RL
5. Calculate XL from $XL = Q.Rt + Xt$
6. Calculate XC2 and XC1 from
$$XC2 = A.RL$$
$$XC1 = \frac{B}{Q - A}$$
where
$$A = \sqrt{\frac{B}{RL} - 1}$$
$$B = Rt(1 + Q^2)$$

The minimum Q calculated is an indication of the probability of success of the circuit design. Ideally the minimum Q should be appreciably lower than the actual Q required. Should the minimum Q be too high, the network is not capable of achieving the required performance. One way of reducing the minimum Q is to use a broadband transformer to reduce the load resistance seen at the output of the network.

Should the load resistance be lower than the real part of the effective transistor load impedance, the program will attempt to take the square root of a negative number when calculating minimum Q. In such cases, the circuit will have to be reconfigured so that an acceptable minimum Q is achieved.

Although, as mentioned previously, the reactance values fed into the program must have the correct sign associated with them, the program output for XC1 and XC2 is positive if these components are capacitive. If any of the reactances calculated by the program are negative, this indicates that it is not possible to achieve a sensible circuit design with the defined parameters.

To ease the readability of the output, it is worth using the fixed decimal format of the calculator to restrict the display to two decimal places.

Analysis program

The flow chart for the analysis program is shown in Fig 3. For this program, the transistor load impedance must be entered in parallel form and, as for the design program, the sign convention for the reactive portion must be observed. The frequency information is only used in ratio form so that the actual units do not matter; ie 2MHz can be entered as 2 or 2000000 or anywhere in between—the only requirement is that both frequencies must be entered in the same units.

Worked example

The worked example below illustrates the use of two programs, it can also be used to prove that the program has been entered correctly. A 2N5070 is to be used to deliver 25W to a 50Ω load using a "T" network tank circuit. The operating frequency range is to be 28 to 29·7MHz and the loaded Q is to be 10 at the design centre frequency of 28·5MHz. A 28V supply is to be used and the transistor's $V_{CE(SAT)}$ is 2V.

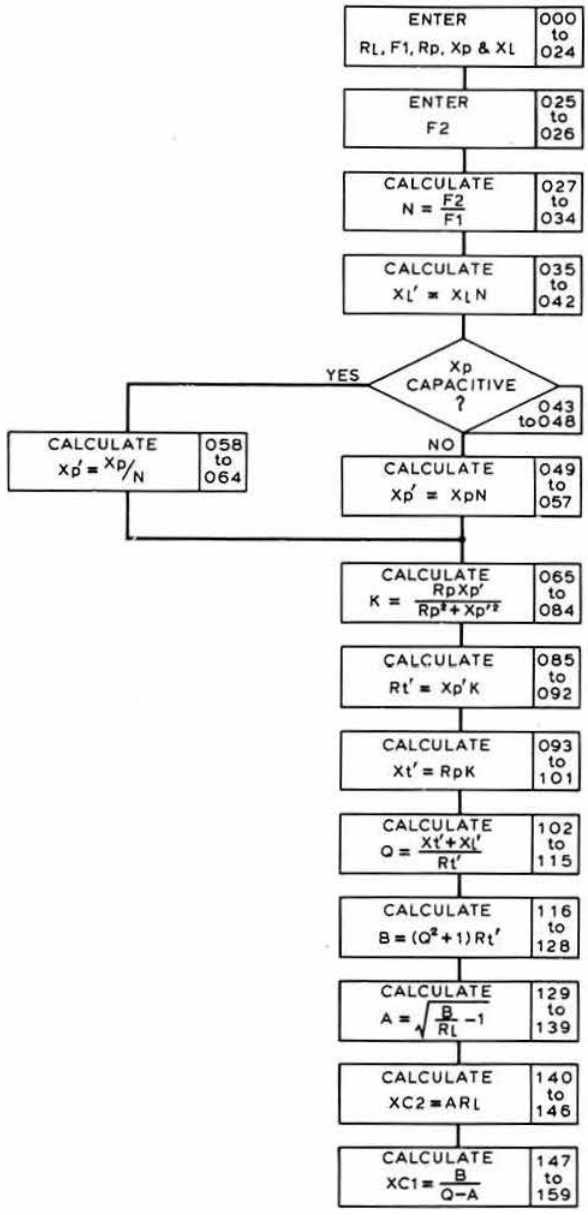

Fig 3. Analysis program flow chart

First calculate

$$RP \text{ from } Rp = \frac{(V_S - V_{CE(SAT)})^2}{2W} = \frac{26^2}{2 \times 25} = 13{\cdot}52\Omega$$

From the data sheet for the 2N5070 the output capacitance is 170pF at 28·5MHz, ie Xp = −32·85 at 28·5MHz.

Having established the basic data above, the design program can be used to determine the values of the components. The minimum Q is the first parameter calculated; this, for the example, is found to be 1·82. Since this gives a reasonable margin

compared with the required Q, calculations for X_L, XC1 and XC2 can be carried out. The results achieved are: $X_L = 120{\cdot}37$ ($L = 0{\cdot}672\mu H$), XC1 = 221·50 (C1 = 25·21pF7) and XC2 = 236·40 (C2 = 23·62pF). If required, the calculations can be repeated for different values of Q, RL, Rp or Xp.

With a satisfactory design having been achieved, the effects of parametric variations can be established using the analysis program. The results of a series of calculations are summarized in Table 2; obviously additional calculations could be carried out, if required, to yield the worst case minimum and maximum values for C1, C2 and Q. If the results are satisfactory, appropriate components can be chosen and the circuit constructed.

Conclusions

The run time for the design and analysis as presented above, including manual program loading, was about 15min. As can be seen, an appreciable amount of information has been gained for very little expenditure of time. Also, perhaps more important, the constructor will have a high confidence in the successful operation of the circuit when it has been built.

Detail listings for the programs, appropriate to the TI58/59 series of calculators, are available from the author (on receipt of an sase). By reference to the flow charts, Figs 1 and 2, the programs can easily be rewritten for other scientific programmable calculators or for a home computer. To give some idea of the store requirements, the design program uses 132 steps and nine data registers, and the analysis program uses 160 steps and 14 data registers—these figures being for the TI58/59 calculators. □

Table 2. Analysis program results

INPUT				OUTPUT				
Freq (MHz)	RL (Ω)	Cp (pF)	Xp (Ω)	Q	XC1 (Ω)	C1 (pF)	XC2 (Ω)	C2 (pF)
28				9·77	218·02	26·07	231·45	24·56
29·7				10·56	229·74	23·33	248·38	21·57
28		340	−16·43	13·66	186·70	30·45	272·28	20·88
29·7		340	−16·43	15·24	195·56	27·40	297·32	18·02
	33			10	280·29	19·92	194·44	28·72
	75			10	188·85	29·57	286·26	19·51

Q variation = 9·77 to 15·24
C1 variation = 19·92 to 30·45pF
C2 variation = 18·02 to 28·72pF

Notes: 1. Blank input entries mean that the nominal value is used.
2. Xp is the reactance of Cp at the nominal frequency (28·5MHz).

An 80-channel selector system for the IC240

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Introduction

Having acquired an IC240 for mobile use, the author gave some thought to the possibility of increasing its capabilities for fixed station use, particularly when not QTHR. The accessory described below was not intended for mobile use, as a change in frequency is not easy to implement without looking at the switch positions; with the inevitable distraction from the road when mobile.

Design

Examination of the circuit diagram and the diode matrix tables indicated that a binary coded input was required on the coding input lines, with a lowest input N of 64. The input N is increased by one for every 25kHz step above 144MHz. The section of the IC240 circuit diagram used for the addition of the duplex shift gave a good indication of a method by which a logical system of switching could be utilized, and the addition of binary numbers achieved to obtain the correct inputs to the coding lines.

The circuit (Fig 1) was designed from basic principles, and the choice of cmos devices was made to ensure compatibility with the existing IC240 circuit elements. An added bonus is a saving in cost and complexity in respect of voltage regulation; this would have been necessary if ttl packs had been used, with little saving in device costs.

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Construction

The circuit was designed for use with three single-pole rotary switches, which were used to select and display: units of megahertz, switch A; hundreds of kilohertz, switch B; and twenty-fives of kilohertz, switch C. The author preferred this "frequencies" method of presentation rather than channel numbering. The UK standard of having no designated channel numbers below 145MHz, and channel zero starting at 145MHz, inhibited the channel method of presentation. (The frequency channels below 145MHz are required for Raynet groups, which also use the "beacons only" section of the band) [1].

Any constructor wishing to use rotary switches for selection and indication, should use the entire circuit. The switches are wired through the diodes, in the positions indicated in the circuit diagram, to the printed circuit board (Fig 2) which has its inputs coincident with points A4, A1, B8, B4, B2, B1, C2 and C1 of the circuit diagram. The use of bcd thumbwheel switches will allow for dispensing with all the diodes, shown within the dotted lines on the circuit diagram, which are external to the pcb. The connections from the switches to the pcb are made directly to points A4 to C1, respectively, from the appropriate bcd outputs of the switches.

The 9V line should be connected to the rotary switch wiper tag or the thumbwheel switch common terminal from the input side of the pcb. The output points of the pcb are connected via a multiway flexible cable to the nine-pin accessory plug. The nine-pin socket at the rear of the IC240 has the centre zero meter lead and the earth connections removed. The active lead